

ar deposited on the exposed portions of layers 52, 54, 56, 58 and 60 as well as the dielectric layer 70 and exposed regions of Cu in the metallization level 30.

(9) Please replace the sentence at page 8, line 1 with the following rewritten

99 sentence: A lower conductor level 30 includes a runner portion 123 effecting connection between lower plate 52 and a via portion 92 of level 40.

(10) Please replace the sentence at page 8, line 8 with the following rewritten

100 sentence: Connections to individual layers 122 are made through via portions 126 and conductive runners 120, 123 and 125 to configure four capacitors connected in parallel.

IN THE CLAIMS

1. **(Amended)** A monolithic integrated circuit comprising:

at least first and second levels of interconnect conductor for connection to a semiconductor layer; and

911 a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane and formed between the first and second levels of conductor, including

a first conductive layer,

a first insulator layer formed over the first conductive layer,

a second conductive layer formed over the first insulative layer ,

a second insulator layer formed over the second conductive layer, and

a third conductive layer formed over the second insulative layer,

with the first and third conductive layers commonly connected.